REMARKS

Claims 1-2 were rejected under § 102(b) over Tottori '680. This rejection is respectfully traversed. Amended claim 1 recites

A semiconductor device, comprising:

exposed fuse terminals provided adjacent a chip substrate surface; and

an exposed discharge contribution terminal which is provided adjacent said chip substrate surface;

wherein a first height, from said chip substrate surface to a top face of said discharge contribution terminal, is higher than a second height, from said chip substrate surface to a top face of said fuse terminals.

Sparks. Instant Fig. 12 shows the problem solved by the invention, the possibility of a spark 246 to the fuse terminal 234, which, unlike the chip terminals 232, is unprotected against such static discharge (page 6, lines 23-27). Adding static discharge protection to the fuse terminals would take up chip area (page 7, lines 4-11), so a new solution has been needed (page 7, line 12-17).

The Applicant conceived the claimed discharge contribution terminal which is *higher* than the unprotected fuse terminals. Like a lightning rod, it will attract sparks before they hit the unprotected fuse terminals. Electrostatic damage is prevented (page 17, lines 9-17).

Well Region 4. The Examiner asserts that Tottori discloses a chip terminal 16 which is higher than a fuse terminal 4. However, Tottori itself refers to element 16 as a "fourth interconnection layer" (¶[0062]) and it refers to element 4 as a "well region" (¶[0053]) in the discussion of Fig. 1 (which also describes applied Fig. 6; see ¶[0096]). The well region 4 is shown in Fig. 6 to be sunk into the substrate 1, where it cannot possibly act as a terminal.

A Non-Applied Element. In applied Fig. 6, the only element which is at all comparable to the fourth interconnection layer 16 is the third interconnection layer 14, but this element 14 is buried inside an insulation film 24 (see ¶[0061] and applied Fig. 6). Clearly, the layer 14 cannot possibly act as the claimed "terminal" if it is buried in insulation. Therefore, the applied Fig. 6 shows exactly *one* possible terminal, and not the two different terminals that are claimed.

Claim 1 is amended to recite that the terminals are exposed, which is believed already to have been inherent in the word "terminal." Claim 1 now further distinguishes over Tottori.

The non-applied interconnection layer 14 includes two contact portions 12 which span the fuse 13 (see Fig. 2). Overcurrents through the layer 14 are used to blow the fuse 13 (¶[0066]). The layer 14—as is shown in applied Fig. 6—is not a fuse terminal because, as noted above, it must be exposed to the outside. No actual fuse terminal is disclosed. While there must be some way to send currents through the layer 14, Tottori is not concerned enough with any actual fuse terminals to illustrate or describe them. (No disclosure of any fuse terminal is admitted.)

No Exposed Terminal Disclosed. Furthermore, the Applicant respectfully submits that even element 16 is not a "terminal" because it is not disclosed to be one—with respect, the Examiner has only *inferred* that it is a terminal, from applied Fig. 6 in which it lies on the surface. Tottori is not seen to refer to element 16 as a "terminal" anywhere. Layer 16 has the same structure as the buried layers, and it seems likely to the Applicant that any actual terminal would be larger in area, and more robust, than a buried wiring layer.

No Exposed Discharge Contribution Terminal is Disclosed. Furthermore, applied Fig. 6 shows that the fourth interconnection layer 16 is coupled directly to the MOS transistor MT (¶[0008]), without any intermediate spark protection, so that a static discharge spark applied directly to element 16 would probably blow the transistor. Therefore, element 16 is not the "discharge contribution terminal" that the Applicant claims in claim 1, even if it were a terminal.

The subject matter of new claim 5 is completely lacking from Tottori.

Thus, of Tottori's asserted"terminals" 16 and layer 14 (no anticipation is admitted), one is buried in insulation and can neither be a terminal nor be exposed to static electricity, while the other is highest but is coupled directly to a transistor and therefore provides no protection, even though it will attract the sparks. With respect, there is no anticipation.

Claim 6. Claim 1 recites that the height of the discharge contribution terminal from the chip substrate surface to the top face is higher than the top face of the fuse terminals, and the subject matter is exemplified in the specification at page 8, lines 6-7, which explains that "top face" refers to the surface of the formed bumps. According to this, each of the fuse terminals and the discharge contribution terminals has a bump.

No bumps are disclosed by Tottori, and there is no anticipation of claim 6.

Claims 3-4 were objected to as dependent but being allowable. These claims are rewritten as new claims 7-8.

Reconsideration and allowance of all claims is requested.

Respectfully submitted,

June 6, 2005
Date

Nick Bromer (Reg. No. 33,478)
(717) 426-1664
RABIN & BERDO, P.C.
CUSTOMER NO. 23995
Telephone: (202) 371-8976
Telefax : (202) 408-0924